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FOR
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ON
DC TO DC CONVERTER
ENGINEERED MAGNETICS MODEL EMCR131
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NOTE

Within this report, reference is made to Engineered Magnetics proprietary circuits. These circuits were developed during a company sponsored R & D program prior to the initiation of this study contract. In the best interest of the unit being designed under this study, it is the intention of Engineered Magnetics to utilize these proprietary circuits in the Pulse Width Regulator. Patents for these circuits are being applied for at the present time.

SUMMARY AND CONCLUSIONS

This report covers the second phase of design of a highly efficient DC to DC Converter with 59-watt output consisting of 4 regulated, isolated, and short circuit protected outputs. The initial report submitted, covering the first phase of design, discussed the study of an overall "block diagram" approach consisting of the construction of an oscillator and pulse width regulator section, and a search for a transistor for use as a suitable synchronous rectifier. This type of transistor is currently not available and it appears unfeasible to be fabricated under present transistor technology. This is due to two incompatible requirements of high base-emitter voltage and fast switching times.

During this second period, more time was expended on optimizing the pulse width regulator than was anticipated at the completion of the first period of work. Consequently, the development of the output series regulator and current limiting circuitry that was to be designed during the second period was not completed. However, design effort has been directed toward these circuits and a preliminary design is near completion. Little difficulty is anticipated here, and this circuitry will be completed in the next phase of work.

I. INTRODUCTION

This report describes the second quarterly period of effort to develop a DC to DC converter of very high efficiency.

During this second phase of work, satisfactory synchronization of the master and boost oscillators was accomplished. Subsequent to that, the largest portion of the time was spent in an attempt to increase the efficiency of the pulse width regulator supplying input power to the boost oscillator. Three other types of regulators were built and tried. Each type presented certain problems that resulted in an overall lower efficiency for the converter as a whole. It was decided that the original approach was superior and effort was concentrated on optimizing this design. The preference of the first approach was further enhanced by the recent introduction of a high speed, high beta, high current, low saturation resistance PNP silicon transistor by Motorola.

The entire pre-regulating circuitry, consisting of the main and boost oscillators and the pulse width regulator, has been tested and found to work satisfactorily. Pre-regulation ahead of the output series regulators can be held to ±2% over the entire input voltage range.

As discussed in the first quarterly report, the basic circuitry to regulate for input voltage variation is shown in Figure 1.

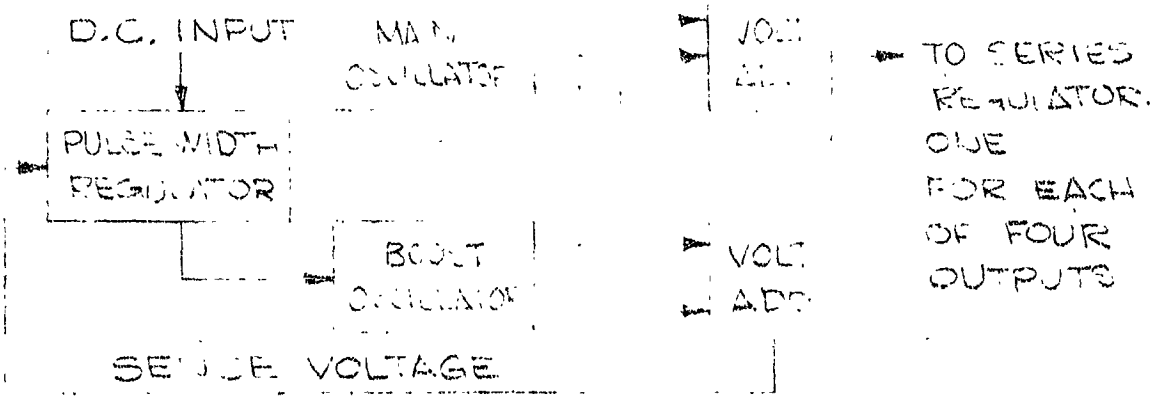


FIGURE 1. BLOCK DIAGRAM OF DESIGN APPROACH.

II. DISCUSSION

At the end of the first period of effort, some difficulty was experienced in the synchronization of the two power oscillators (main and boost). This problem was corrected at the beginning of this reporting period. The method of driving the boost oscillator transistors from the base circuits of the main oscillator transistors was used instead of the collector circuit method as described in the last report. The entire pre-regulating circuitry was tested and found to work satisfactorily. Efficiency from the input to the series regulators (not including series regulation) was approximately 88%. Efficiency is almost independant of input voltage. This indicates that as the input voltage increases, the increase in efficiency of the main oscillator is just offset by the decrease in efficiency of the P.W.R.-Boost Oscillator combination.

A. PULSE WIDTH REGULATOR

The pulse width regulator that is being used is shown in Figure 2.

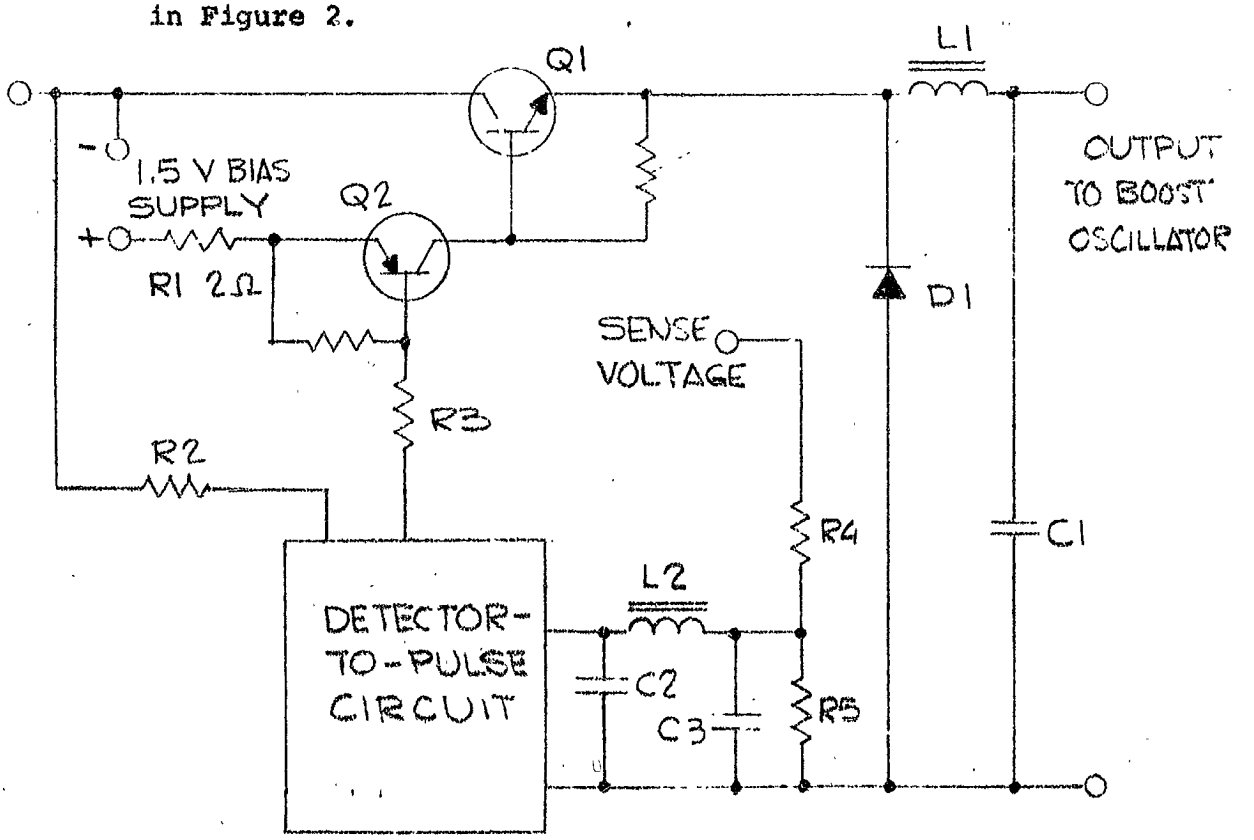


FIGURE 2 PULSE WIDTH REGULATOR SIMPLIFIED CIRCUIT

The series switch Q1 is driven by Q2. Transistor Q2, in turn, is controlled by the Detector-to-Pulse Circuit. This circuit is designed to switch from one state to the other with a minimum voltage change. If the sense voltage rises, the Detector-to-Pulse Circuit is turned on and hence Q2 and Q1 are turned off bringing the sense voltage back to the desired level. The commutating diode D1 discharges L1 when Q1 turns off. L1 and C1 form the output filter. Note that the frequency of switching is not fixed but is a function of L1, C1, and the load.

There are some inherent problems and disadvantages associated with this circuit.

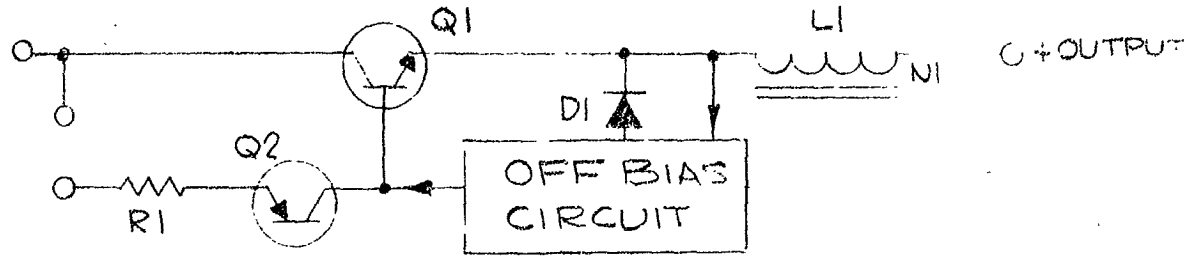
1. Bias Supply

   First, a separate bias supply must be included to insure that Q1 is completely saturated. This bias supply must be a regulated voltage. This can be seen from the following consideration. The bias voltage must be at least 1.5 volts and supplies 200MA of drive power to Q1. This is a total of 300 MW when Q2 is on. If the bias voltage is a function of the input voltage, it would have to be designed to be 1.5 volts when the input voltage is at its minimum of 12 volts. When the input voltage is at 20 volts, the bias supply voltage would be $\frac{20}{12}$ (1.5) = 2.5 volts. The additional volt would appear across R1 which would raise the current from 200MA to 700MA. The bias power when Q2 is "on" would now be (2.5)(.7) = 1.75 watts. Even though Q2 and Q1 are "on" a decreasing percentage of time as the input voltage increases, this still causes a prohibitive power loss. Thus the bias supply must be coarsely regulated. It is derived from additive windings in the two power oscillators in the same manner as the four outputs and the sense voltage for the P.W.R. It thus requires two separate

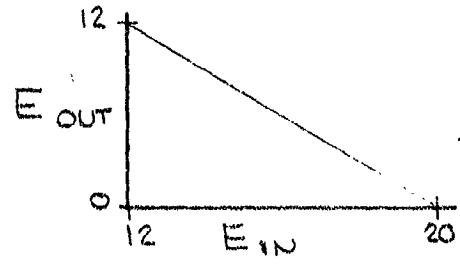
bifilar windings, four diodes, and a capacitor to generate the bias supply. The rectifying diodes account for another 100MW of loss.

2. Q1 Turn Off

Another problem of the circuit is that there is no practical method of turning Q1 off quickly with a negative base current pulse. The method is to put an Off Bias Circuit on L1 to provide a negative bias on the base of Q1 when it starts to turn off. The circuit is the following:



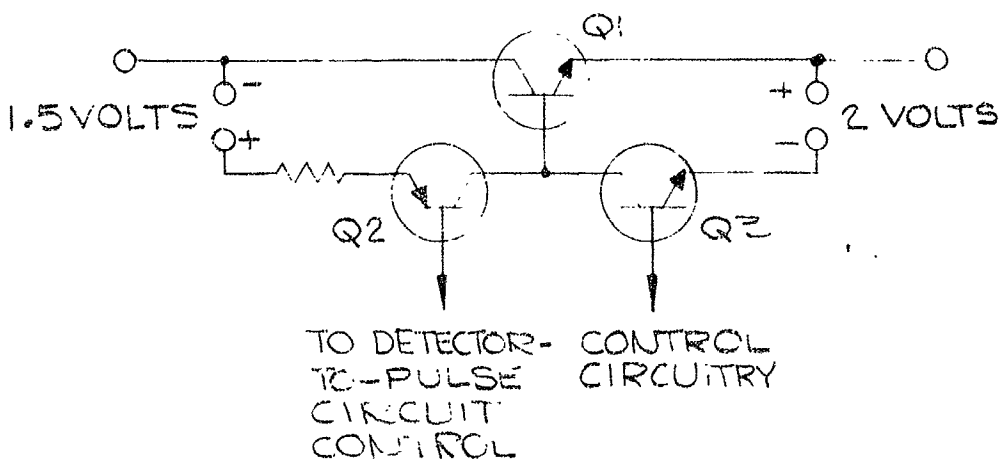
This method works very well when the output voltage is constant. Under this condition the voltage across N1 of L1 is always the same value when Q1 is off and L1 is supplying power to the output. Specifically, the voltage across N1 equals the output voltage plus the voltage drop across D1. With a fixed voltage across N1, it is an easy matter to design the Off Bias Circuit to give the proper turn off drive. However, in the circuit being used, the output voltage is not constant but varies from about 12 volts down to almost zero volts as the input voltage goes from 12 volts to 20 volts. The ideal characteristic of the regulator is the following:



$$E_{OUT} = 30 - \frac{3}{2} E_{IN}$$

$$12 \leq E_{IN} \leq 20$$

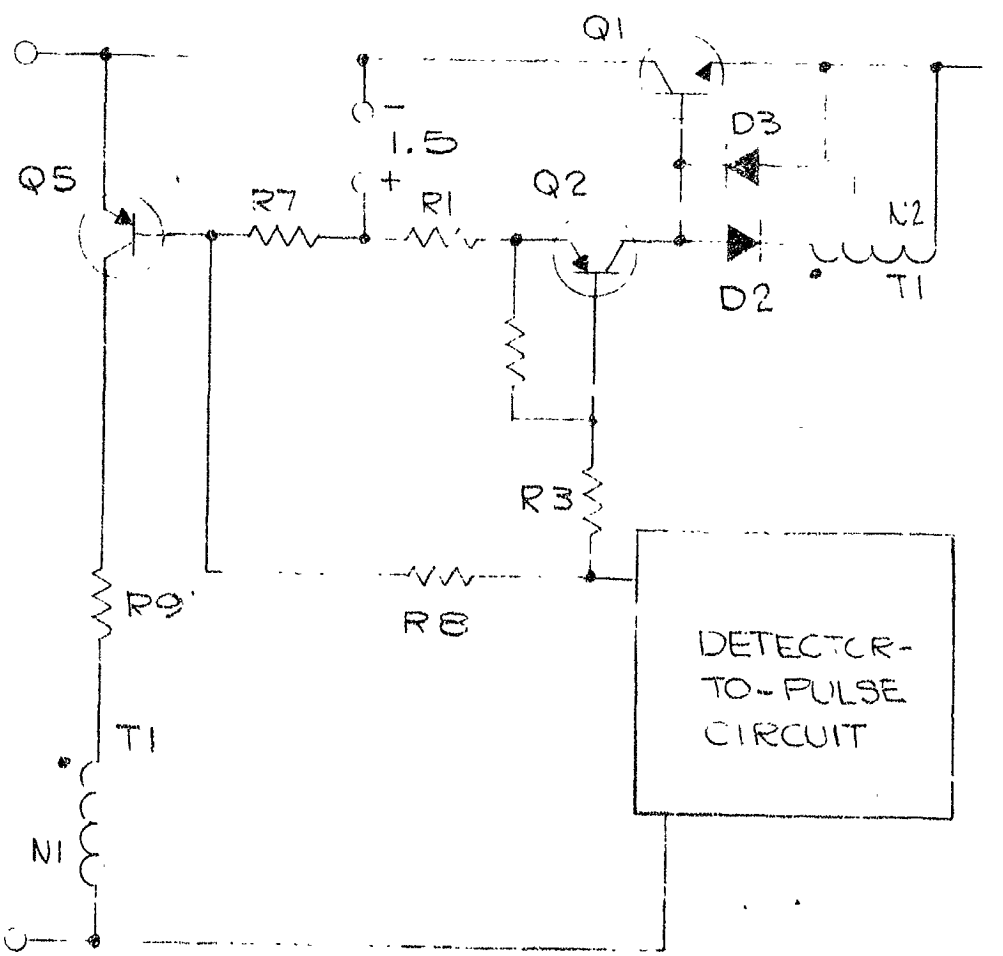
With this mode of operation it is impossible to design a feasible Off Bias Circuit. Other methods were tried, such as connecting the base of Q1 to a negative voltage with respect to the emitter of another transistor in the following manner:



This system did not prove feasible because of the added control circuitry that was needed in addition to Q3 having to carry a moderate amount of current and turn on very fast. Q1 is a Minneapolis-Honeywell 2N2812 and is capable of turning off in 50ns with the proper turn off drive. The control circuitry to turn Q3 on-and-off is very complicated since the emitter of Q3 is at a potential almost equal to the output voltage when it begins to turn on and rapidly decreases to about one volt below the common bus as Q1 turns off. Since the output voltage varies from 12 volts down to zero, this means the power to turn on Q3 must come from a source of 13 volts or more. When the emitter of Q3 drops

to minus one volt when Q1 turns off, the base current for Q3 comes from at least a 13 volt source. To prevent prohibitive losses, the turn on signal for Q3 would have to be of a short duration and extremely fast rise time. The complexity of the circuitry needed to accomplish this eliminated the use of this type of turn off drive.

3. Another approach attempted was to charge a linear powder core from the input source and then open it and let the energy stored in the core provide the turn off bias. The circuit used was the following:



When the Detector-to-Pulse Circuit operates, Q5 is turned on through R8. When Q5 turns off, the collapsing field in T1 provides a negative bias on N2 to turn off Q1. R7 returns the base of Q5 to the positive bias to give quick turn off of Q5. Diode D3 is for the purpose of allowing T1 to discharge after the stored charge has been cleared from the base of Q1. Before the charge has been removed, the back voltage drop across the base-emitter junction of Q1 is less than the forward diode drop, therefore no current flows through D3 until Q1 is off. This approach worked in that it achieved faster turn off of Q1. However, it did not accomplish an increase in overall efficiency. One reason is that the frequency of switching of the regulator varies from about 1KC to 5KC over the load range. At the lower frequencies, T1 saturates early in the cycle and the maximum current flows through R9, Q5, and N1 for 80% of the time. Another problem is that Q5 must turn off much faster than Q1 if it is to do the most good.

Attempts will be made in the next phase of work to determine just how much power is lost in Q1 due to a turn off time of 0.3μs instead of 50ns. It appears now that the power lost due to this is small enough considering there is no circuitry which, in itself, is efficient enough to save this power.

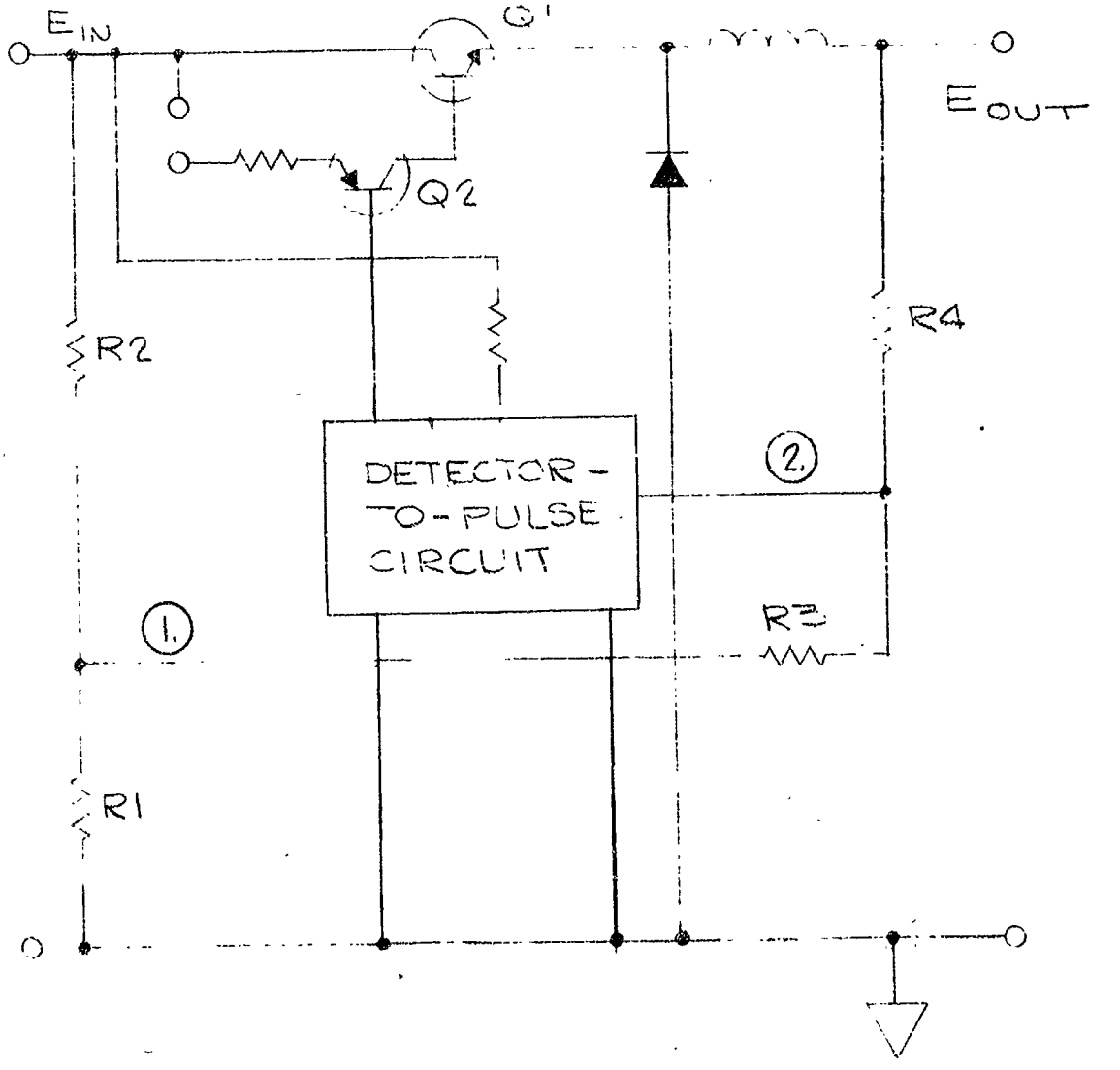
4. Feed Back Loop and Zero Output Voltage

A problem always encountered in any regulator that has a low voltage output is ripple. The ripple problem in the regulation circuit being used is complicated by two factors. First, the output voltage is not the voltage that is being sensed. As the output voltage varies over the range of 12 to 0 volts, the sense voltage remains constant at 12 volts. It is the sense voltage that the regulator is regulating. It is at the sense point that

percentage ripple is measured as far as the regulating circuit is concerned. The absolute p-p ripple then remains constant so that as the output voltage decreases, the percentage ripple increases. Secondly, the p-p value of the ripple is fairly large to begin with. It must be remembered that the feed back control loop for the regulator contains two DC-DC converters whose outputs are connected in series to form the sense voltage. The trade off that must always be made between output ripple and regulator frequency response becomes extremely difficult for this circuitry. The pi filter consisting of C2-L2-C3 was determined empirically and the breadboard operates satisfactorily. However, further analysis will be accomplished in this area to insure proper operation in a production situation. In addition, good filtering is needed between the output of the regulator and the input of the boost oscillator. This is because the ripple on the output of the regulator is approximately 300mv p-p. The frequency of the oscillator is 4KC. The frequency of the regulator varies from 1KC to 5KC as the load varies. If the frequency of the regulator happens to be very near 4KC and the output voltage is low so that the percentage ripple is high, the result is that one of the switching transistors in the boost oscillator sees a higher net DC input voltage than the other one. This causes a non-symmetrical wave shape in the boost oscillator which drives the core into saturation on one-half cycle. The "roundness" of the B-H loop of the supermalloy cores being used minimizes this problem, but additional filtering is still used between the regulator and boost oscillator.

B. OTHER REGULATOR APPROACHES

Other regulator circuits were studied to minimize or eliminate some of the problems mentioned above. In order to eliminate the problems of oscillation and response time in the feed back loop, an open loop regulator was tried. As was stated earlier, the ideal relationship between the input and output voltages of the regulator is $E_{out} = 30-3/2\ E_{in}$. The following circuit was designed to provide this function:



The operation of the circuit is as follows. The point of regulation or constant voltage is the sense point of the Detector-to-Pulse Circuit. The voltage at this point is equal to

1) $E_{in}\left(\frac{R1}{R1 + R2}\right) + \left(E_{out} - \frac{R1}{R1 + R2} E_{in}\right) \frac{R3}{R3 + R4}$

This equation is true if it is assumed that the current through R1 comes entirely through R2. That is R2 is much less than R3 + R4. This is easily made valid since the sense point is $\approx$ 10μa and the current through R1 and R2 can be made 100 times this large without an appreciable power loss.

If we now let

2) $K_1 = \frac{R1}{R1 + R2}$ $\qquad$ $K_2 = \frac{R3}{R3 + R4}$

and solve for K1 and K2 from the boundary conditions, we get

3) $K_1 E_{in} + (E_{out} - K_1 E_{in}) K_2 = E$ sense

E sense was chosen to equal 6 volts.

The boundary conditions are

when: E_{in} = 12 volts, E_{out} = 12 volts

E_{in} = 20 volts, E_{out} = 0 volts

E sense = 6 volts

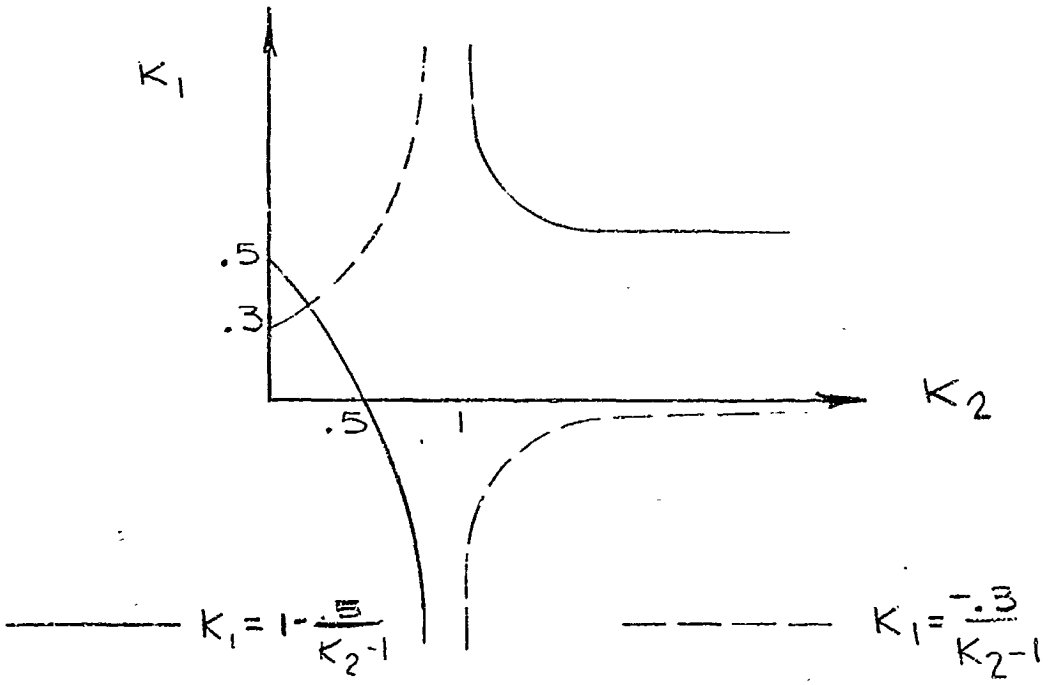
Inserting these conditions into equation 3) above derives the following two equations:

4) $12K_1 + (12 - 12K_1) K_2 = 6$

5) $20K_1 + (0 - 20K_1) K_2 = 6$

from 5) $K_1 = \frac{-}{\quad - 1}$ $\qquad$ from 4) $K_1 = 1 - \frac{.5}{K_2 - 1}$

The graph of these two equations is shown in the following figure:



There are two solutions, but the one at $K_2 = 1$, and $K_1 =$ infinity is indeterminate. The root at $K_1 = \frac{3}{8}$, $K_2 = .2$ is the usable root.

The regulator that was built had

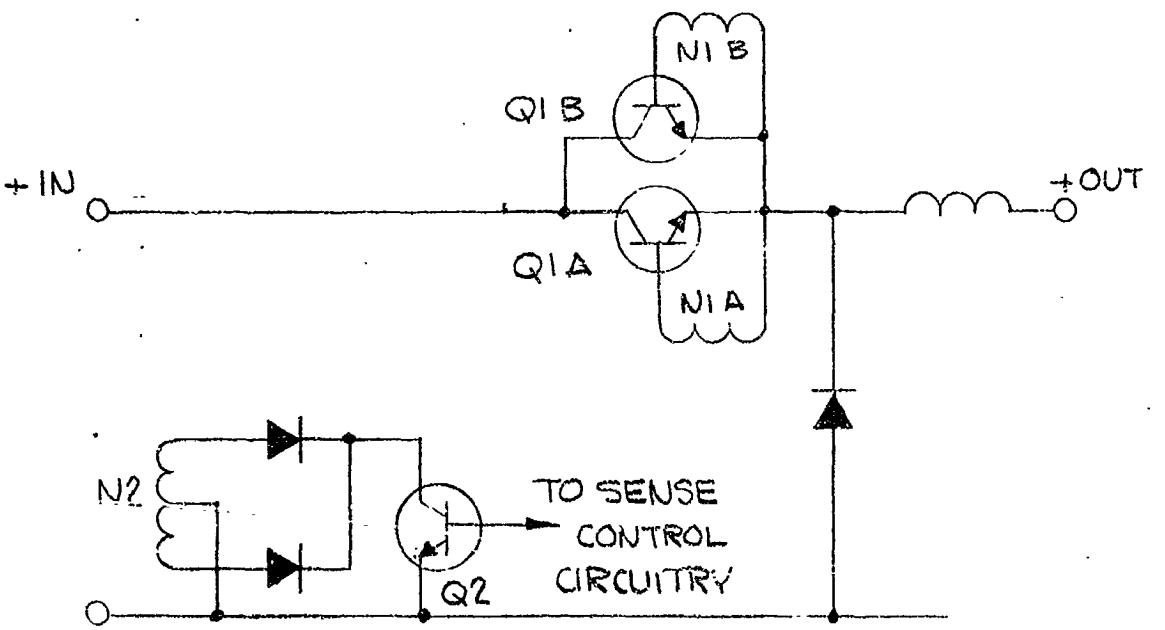
R1 = 1.5K, R2 = 2.5K, R3 = 10K, R4 = 40K

The overall performance was very close to what was anticipated. One large drawback was that the output voltages ahead of the series regulators could not be held to a tight enough tolerance over temperature. Even with temperature compensating circuitry in the regulator, performance could not be made much better than ±5%. This added percentage (±2% can be achieved with closed-loop regulation) means that 3% less efficiency would be obtained with this open loop regulation method! The importance of holding this pre-regulated voltage to as tight a tolerance as possible is emphasized by the fact that the Honeywell 2N2912 transistors that are being used for series regulators can operate over the entire temperature range with less than 0.3 volts collector-

emitter voltage. The added voltage drop that must be inserted ahead of the series regulator need only be large enough to allow for load transients. The amount of extra voltage that is needed is a function of the magnitude of the step load change, the response time of the regulator, and the size of the filter capacitor ahead of the series regulator.

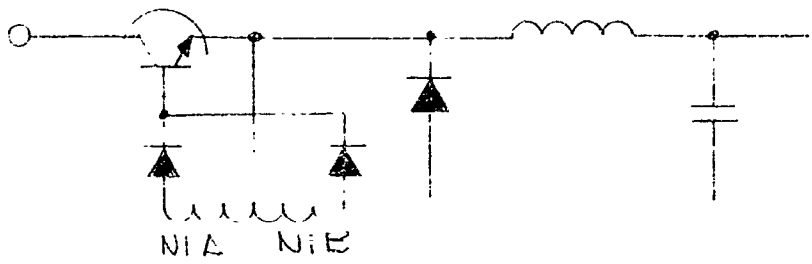
C. CURRENT DRIVEN REGULATOR

A current driven regulator circuit was tried in order to eliminate the losses inherent in a fixed bias supply for Q1. The basic circuit concept was the following:



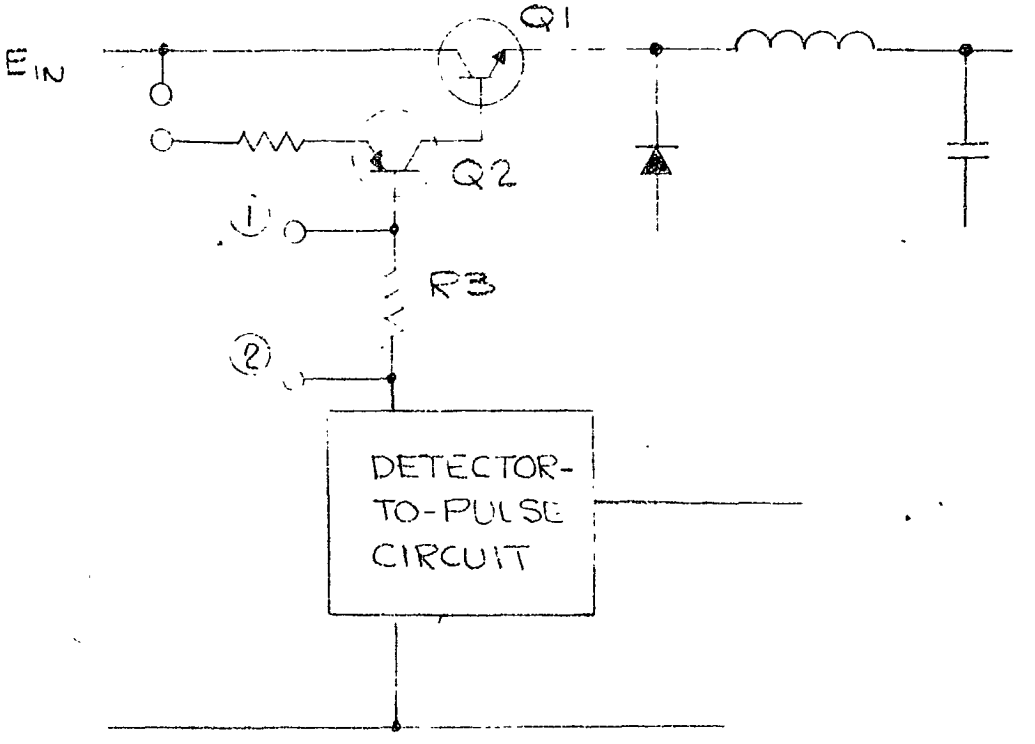
N1 and N2 are secondary windings of a current transformer whose primary windings are placed in the collector circuit of the main power oscillator in the same manner as the current transformer that pr /ides base feed back power. When Q2 is open, power is fed in alternate half-cycles to either Q1A or Q1B that closes the series switch. When Q2 is turned on, the current transformer is shorted and Q1A and Q1B are off. The sense control circuitry determines the switching of Q2. Two transistors were

used for Q1 so that rectifying diodes could be omitted in the base drive windings N1A and N1B. The current in the transformer is AC. If only one transistor were used, the drive circuit would have to be a full wave rectified voltage as shown in the following:



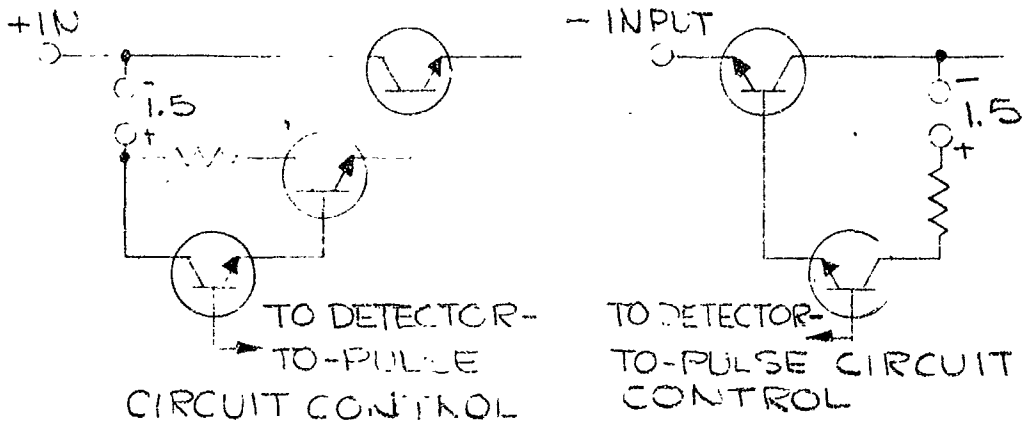
The loss due to the diodes here is about 150mw at full load. The current drive circuit was very efficient in itself. At light load considerable power was saved in base drive. The base current is supplied from a 0.8 volt source (the base-emitter voltage of Q1) instead of a 2.5 volt source as in a voltage driven circuit. This alone saves 340mw at full load. Also, when Q2 is turned on the current transformer is shorted, a condition of almost no loss equivalent to an open circuited voltage transformer. However, the problem which could not be overcome in this circuit was the extremely slow switching times that resulted in Q1. Switching times were on the order of 10ms. The base of Q1 could not be returned to a negative point for turn off because a current transformer can not be connected to a voltage source without losing the whole operation of the circuit. Even though this circuit is considerably more simple and much more efficient in supplying drive power to Q1, it had to be discarded because of the resultant slow switching times in Q1. If a method could be conceived whereby fast switching times could be achieved with this circuit, it would be by far the best circuit to use.

D. Having decided that the original design of the pulse width regulator would have to be used, attempts were made to optimize this circuit. One major source of power loss was the base current for the driver transistor Q2. Referring again to a simplified circuit of Figure 2 as shown below:



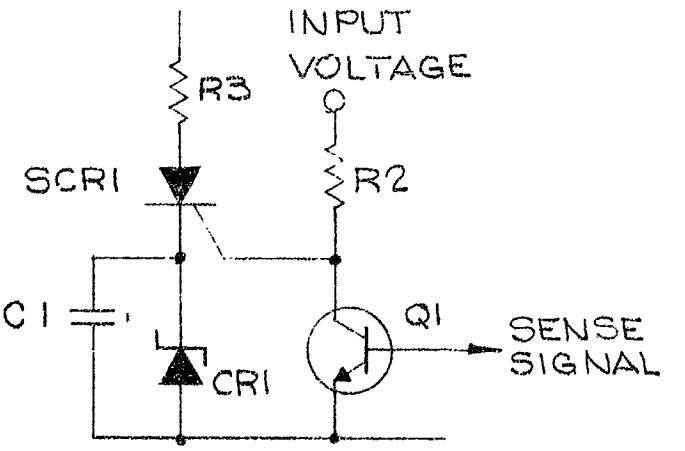
R3 must be chosen to give enough drive to Q2 when E_{in} is at its minimum value of 12 volts. Point (1) in the circuit is nearly always equal to E_{in}. When the Detector-to-Pulse Circuit operates, point (2) is nearly equal to 8 volts. Thus at low input the voltage across R3 is 4 volts. R3 must be chosen to give adequate base current to Q2 under these conditions. At the high input voltage of 20 volts, the voltage across R3 is 20 minus 8 or 12 volts, an increase of 3:1. In the early part of this work period, Motorola 2N2905 transistors were being used for Q2. The minimum drive current needed to give 200MA at saturation was 12MA. At 20 volts input, the base drive

to Q2 is three times as much or 36MA. This current is being supplied directly from the 20 volt input source and therefore represents (36)(20) or 720mw of power when it is flowing. In an effort to reduce this drive current, the darlington circuits as shown below were tried:



In both cases, the resultant increase in switching times of Q1 cancelled any reduction in loss due to less drive power. Toward the end of this work period, Motorola introduced the 2N3025 PNP silicon transistor. This transistor had much higher gain and lower collector-emitter saturation voltage than the 2N2905. Minimum base current to give 200MA of collector current is 3MA. Under this condition only 9MA flows at high input voltage. Since it flows for 12/20 of the time at high line, this represents a power loss of only (.6)(20)(9) = 108mw. This transistor also switches very fast and resultant switching times for Q1 are about 2μs.

One other variation attempted on the original pulse width regulator circuit was the use of a "turn-off SCR" control circuit in place of the Detector-to-Pulse Circuit to convert the analog sense signal into a digital signal to control Q2. The circuit is shown on the following page.

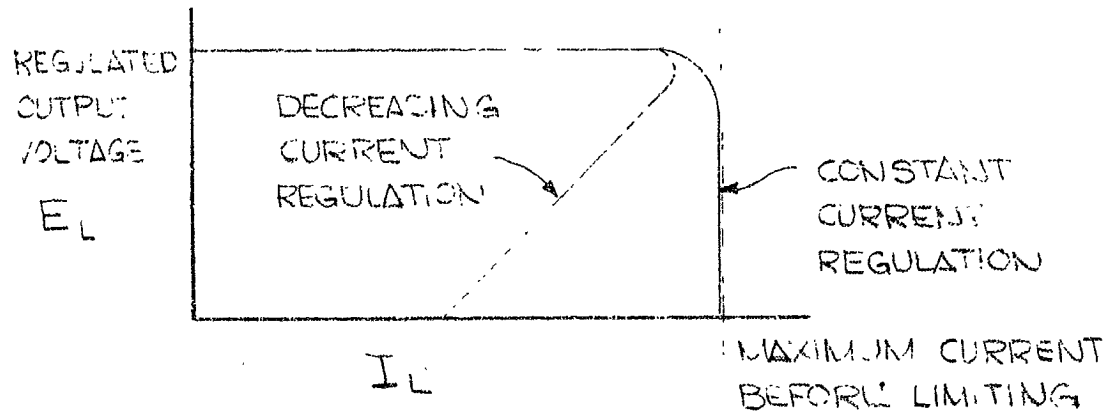


C1 and CR1 maintained a voltage of about 3 volts at the cathode of the SCR. The sense circuitry was designed so that a change of only 30mv at the sense point would change Q1 from off to saturation. When Q1 was off, SCR1 switched on from gate current through R2. When Q1 turned on into saturation, the gate of SCR1 is at 0 potential and the cathode is maintained at +3 volts by C1. The back bias on the gate then turns off SCR1. This circuit worked moderately well. The SCR (Texas Instruments 2N3001 series) switched on with adequate switching speed. Turn off time was slower but still tolerable. One problem that was encountered, however, was sporadic switching. The SCR is extremely sensitive. At high temperature it becomes easier to turn on and harder to turn off. The circuit worked at high temperature even though some false triggering was occurring. The circuit, though, did not offer any obvious advantages over the original Detector-to-Pulse Circuit. Consequently the original circuit was used.

III. PROPOSED PROGRAM FOR NEXT REPORTING PERIOD

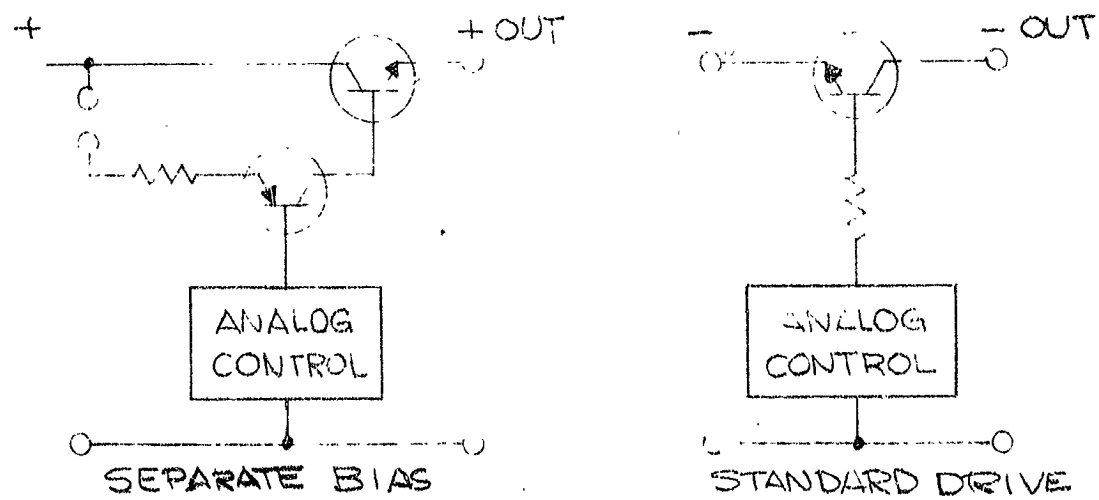
During the next phase of work, the series regulator and current limiting circuitry will be added. This will essentially complete the electronic design. The series regulator circuit will be of a standard design. Only two areas of the unit design are undetermined. One is the type of current limiting

action. One type of current limiting supplies a fixed maximum current as an increasing overload lowers the output voltage. A second type reduces the output current concurrently with a decreasing output voltage. These two characteristics are shown graphically below.



A third method of current limiting that can also be used is a form of "cut-off" in which both the output voltage and current go to zero when the load exceeds a specified value.

The other area of unit design yet to be determined is the type of drive for the series regulator transistors. The two types under consideration are a separate bias supply and a standard drive supply. These two circuits are shown below.



The separate bias offers the advantage of supplying base drive for the series regulator transistor from a 2 volt source instead of from a source equal to the output voltage. However, the added complexity, four diodes and two transformer windings on each power transformer for each of the four separate outputs, of this type of drive seems to prohibit its use. Effort is presently being made in conjunction with Minneapolis-Honeywell to obtain special high gain transistors for the series transistors that will reduce the loss due to base drive to a tolerable figure.